REMARKS

Request For Withdrawal Of Final Rejection

The MPEP describes the conditions under which final rejection in a second office action is proper:

> Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). See MPEP §706.07(a) "Final Rejection, When Proper on Second Action" (emphasis added).

In the present prosecution, the Examiner has introduced a new ground of rejection based on Fruehling in response to Applicant's arguments overcoming the reference of Bickel. Although a minor clairifying amendment was made to claim 1, no amendment was made to claim 17, and the previous rejection has been withdrawn for both based on Applicant's comments. Applicant therefore respectfully requests that the current final rejection be withdrawn.

Claim Rejections 35 U.S.C. §103

Claims 1-8, 13-14, and 16-28 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Danielsen in view of Fruehling.

The rejection of claims 1 and 17 is respectfully traversed. As noted by the Examiner, Danielsen fails to explicitly disclose a buffer collecting asynchronous input variables from I/O circuits. More significantly, however, Danielsen fails to disclose a buffer configured to buffer the input variables to a single location and then provide them to the two processors at the same point to accommodate asynchronicity in the changes of the input variables. Generally, Danielsen fails to teach a practical method of coordinating two redundant processing units that, rather then monitoring a slowly varying single quantity such as wheel speed, must deal with possibly hundreds of inputs that change abruptly and discontinuously (such as binary inputs) that collectively define a state that can change extremely rapidly. Perhaps more fundamentally, Danielsen fails to teach how to coordinate two processors facing rapidly changing states without slowing the processors so much that real-time control can no longer be effected.

Fruehling is cited as teaching a buffer, and although the Applicant is unable to identify a buffer in the Fruehling reference, Applicant acknowledges generally that there are probably

probably memory structures (for example 16) that could function as buffer memories in the Fruehling reference if programmed to do so. Note that the unnumbered triangular element in Fig. 2 of Fruehling labeled as "a buffer from output drive pin" is not a "buffer" as would be required under the present claims which clearly referr to a memory and not an amplifier structure.

Nevertheless, Fruehling does not appear to teach a:

> coordinator program providing each of the first and second processing units with identical copies of the input variables from the buffer at a predetermined point in the repeated execution of the common safety programs

as required by both claims 1 and 17 (in the latter case, as a step).

The Examiner cites column 11, lines 16-24 of Fruehling for this "coordinator program" however this section of the Fruehling reference appears to only teach that two processors get all of the same inputs (something that would be necessary in any redundant processing situation) not that asynchronous variables are collected in a buffer and then at a predetermined point in the repeated execution of a common safety program, delivered to the two processors. The language cited by the Examiner in Fruehling is consistent with both processors receiving a single input variable asynchronously at various different times during the execution of a common safety program--as occured in the prior art--or even each processor having its own, rather than a common buffer.

The Fruehling reference teaches away from the use of this buffer structure and system by describing the receipt of "digitized wheel speed information" where the problems of the present invention of possibly obtaining different outputs from the two processors based on asynchronicity of the received data is either less of a problem or no problem at all. The one example of input data described in Fruehling, input wheel speed data, is clearly intended for use in calculating a slowly varying (in comparison to the cycle speed of the processor) change in wheel velocity where asynchronicity in the data would have little or no effect. In this context, the buffer structure of the present invention would provide no benefit.

Thus, individually or in combination, the cited references do not teach the "controller program" of the present invention nor is there any teaching suggestion for modification of these references which are clearly not directed toward a modern, complex industrial control system, but rather an embedded processor for an anti-skid brake system having a simple and well-defined task.

In light of these remarks and amendments, it is believed that claims 1 and 17 are allowable and therefore that claims 1-15 and 18-28, dependent on claims 1 or 17 are also now in condition for allowance and allowance of claims 1-15 and 17-28 is respectfully requested.

Very truly yours,

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